We Claim:

1. A configuration for generating a low-voltage signal proportional to a high voltage present between a source and a drain of a power semiconductor component, the configuration comprising:

a semiconductor body including said power semiconductor component;

said semiconductor body including a capacitive voltage divider having a series circuit formed by a source-gate capacitance serving as a low-voltage tapping element and a source-drain capacitance serving as a high-voltage element;

said power semiconductor component including a source-drain path connected in parallel with said capacitive voltage divider.

2. The configuration according to claim 1, wherein:

said power semiconductor component includes a source zone, a gate area configured above said source zone, a source-gate capacitance and a source-drain capacitance; and

said semiconductor body is formed with a plurality of openings for setting said gate area in order to set a ratio between the source-gate capacitance and the source-drain capacitance.

3. The configuration according to claim 1, in combination with a low-voltage control IC, wherein:

said power semiconductor component includes a voltage sense metallization providing the low-voltage signal; and

said voltage sense metallization is connected to said low-voltage control IC.

4. The configuration according to claim 3, wherein:

said low-voltage control IC includes at least one component selected from a group consisting of an input capacitance and a resistor; and

said component obtains the low-voltage signal.

5. The configuration according to claim 1, wherein:

said semiconductor body includes a voltage sense region with a voltage sense metallization;

said semiconductor body includes a transistor region with a source metallization; and

said semiconductor body includes a contact plug connecting said voltage sense metallization to said source metallization.

6. The configuration according to claim 1, wherein said power semiconductor component is a compensation component.

7. The configuration according to claim 6, wherein said semiconductor body includes a plurality of floating compensation regions.

8. The configuration according to claim 7, wherein said plurality of floating compensation regions are in a pillar form or a spherical form.

9. The configuration according to claim 8, wherein:

said semiconductor body includes a plurality of compensation regions having a conduction type;

said semiconductor body includes a plurality of wells having the conduction type of said plurality of compensation regions; and

said plurality of compensation regions are connected to said plurality of compensation regions.

10. The configuration according to claim 7, wherein said plurality of floating compensation regions are in a pillar form or a spherical form.

11. The configuration according to claim 1, wherein said power semiconductor component is a vertical component or a lateral component.

12. The configuration according to claim 1, wherein said capacitive voltage divider has a dedicated tap or terminal.

13. The configuration according to claim 1, wherein:

said power semiconductor component includes a source zone, a gate area configured above said source zone, a source-gate capacitance and a source-drain capacitance; and

said semiconductor body is formed with a gate insulating layer for setting a ratio between the source-gate capacitance and the source-drain capacitance.

14. The configuration according to claim 1, wherein said power semiconductor component is a power transistor.